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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,766	03/24/2004	Richard Tran	784-P-1-USA	5900
7590 01/09/2006			EXAMINER	
Drummond & Duckworth			SPITTLE, MATTHEW D	
East Tower			ART UNIT	
Suite 440			PAPER NUMBER	
5000 Birch Street			2111	
Newport Beach, CA 92660			DATE MAILED: 01/09/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/808,766

Applicant(s)

TRAN ET AL.

Examiner

Matthew D. Spittle

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 January 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller.

With regard to claim 1, Miller describes a computer system including:

A power supply (Figure 2, item 11);

A memory storage device (where a memory storage device may be interpreted as a hard disk; Figure 2, items 32 – 37) having a plurality of electrical input and output terminals (Miller describes an IDE device as an example; column 9, lines 8 – 11), said electrical terminals including a control terminal for receiving control signals which control recording and transmission of information into and from said memory device (Miller implicitly describes the electrical terminals having a control terminal since he uses an IDE device as an example. Wikipedia shows the IDE (also known as ATA) interface pinout, providing evidence that control terminals are present, namely pins 23, 25, 37, and 38; see table labeled “Parallel ATA pins”).

An electrical harness for interconnecting said electrical terminals with said processor (Miller describes an IDE device as an example (column 4, lines 20 – 23),

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which is connected using a 40 pin ribbon cable, as evidenced in the Wikipedia reference under the section "Parallel ATA Interface.").

A switch box (where a switch box may be interpreted as a key switch; figure 2, item 20; column 6, lines 29 – 33) including one or more manual switches, said switches including a control switch interconnected between said control terminal and said processor, said control switch having a first position allowing control signals to be transmitted from said processor to said memory storage device (where a first position may be interpreted as either positions 1, 2 or 3; column 6, lines 29 – 33; column 6, lines 38 – 50) and a second position for preventing control signals to be transmitted from said processor to said memory storage device (where a second position may be interpreted as OFF; column 6, lines 29 – 33; column 6, lines 38 – 50).

Miller implicitly describes a processor since he describes a personal computer having a motherboard. Both Do et al. (column 3, lines 20 – 22) and van Rumpt (column 1, lines 20 – 26) provide evidence that a processor is included in personal computers that contain a motherboard.

With regard to claim 2, Miller describes the computer system of claim 1, wherein said switch box includes a power switch (where a power switch may be interpreted as a key switch; Figure 3, items 20, 21) interconnected between said power supply and said memory device, said power switch including a first position allowing power to be transmitted from said power supply to said memory device (where a first position may be interpreted as either positions 1, 2 or 3; column 6, lines 29 – 33; column 6, lines 38 –

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50) and a second position preventing power to be transmitted from said power supply to said memory device (where a second position may be interpreted as OFF; column 6, lines 29 – 33; column 6, lines 38 – 50).

* * *

Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Browne.

With regard to claim 3, Browne describes a computer system including:

A processor (where a processor may be interpreted as a central processing unit; Figure 6, item 104a);

A plurality of memory storage devices (where a hard disk drive may be interpreted as a memory storage device; Figure 6, items 122, 110a – 110c), said memory storage devices having a plurality of electrical input and output terminals (Figure 3), said electrical terminals of said memory storage devices including a control terminal (Figure 3, pins 23, 25, 37, and 38) for receiving control signals which control recording and transmission of information into and from said memory device.

An electrical harness for interconnecting said electrical terminals with said processor (Browne describes an IDE device as an example (column 8, lines 29 – 34), which is connected using a 40 pin ribbon cable, as evidenced in the Wikipedia reference under the section “Parallel ATA Interface.”).

A switch box including a plurality of manual switches, said switches including a plurality of control switches interconnected between said control terminals and said

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processor, said control switches having a first position (where a first position may be interpreted as "OUT"; column 9, lines 8 – 13) allowing control signals to be transmitted from said processor to said memory storage devices and a second position (where a second position may be interpreted as "SECURE"; column 9, lines 8 – 13) for preventing control signals to be transmitted from said processor to said memory storage device (column 8, lines 17 – 42).

Browne implicitly discloses the limitation of the computer system having a power supply. It is well known in the art that computer systems operate using electrical power, and therefore furnishing a means to provide this power through a power supply would be apparent to one of ordinary skill in this art at the time of invention by applicant in order for the computer system to be operational.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Browne in view of Henriquez.

With regard to claim 4, Browne fails to teach the computer system of claim 3 having a plurality of power switches interconnected between said power supply and said memory storage devices, said power switches a first position allowing power to be transmitted from said power supply to said memory devices and a second position preventing power to be transmitted from said power supply to said memory devices.

Henriquez teaches a plurality of power switches interconnected between said power supply and said memory storage devices, said power switches a first position allowing power to be transmitted from said power supply to said memory devices and a second position preventing power to be transmitted from said power supply to said memory devices (column 3, lines 14 – 19; Figure 2, items 221 – 224).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the power switches as taught by Henriquez into the switch box as taught by Browne for purposes of controlling power to a plurality of memory storage devices. This would have been obvious in order to gain the ability to “hot swap” the devices as Henriquez teaches in column 3, lines 16 – 19.

Conclusion

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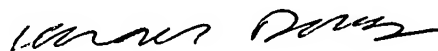
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MDS



Rehana Perveen
Supervisor